


[Web](#) [Images](#) [Groups](#) [News](#) [Froogle](#)<sup>New!</sup> [more »](#)


[Advanced Search](#)  
[Preferences](#)

## Web

 Results 1 - 10 of about **571** for **scan flip-flop master latch slave latch**. (0.24 seconds)

### [PDF] [Lecture 10: Latch and Flip-Flop Design Outline](#)

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... into the flop • Multiplexed or clock **scan** • Crosstalk insensitivity ...  
 5/7/2001 EE371 5 **Flip-Flop** Delay • Sum ... 9 Types of Flip-Flops  
**Master-Slave Latch** D Clk ...

[www-classes.usc.edu/engr/ee-s/577bb/lect.10.2up.pdf](#) - [Similar pages](#)

### Sponsored Links

#### [Latch Hardware](#)

 Huge Variety of Latches & Related Products. Search ThomasRegister.com  
[www.ThomasRegister.com](#)
[See your message here...](#)

### [PPT] [Testing in the Fourth Dimension](#)

 File Format: Microsoft Powerpoint 97 - [View as HTML](#)

 ... D. TC. SD. CK. Q. Q. MUX. D **flip-flop**. **Master latch**. **Slave latch**. CK. TC. Normal mode, D selected. **Scan** mode, SD selected. **Master** open. **Slave** open. t. t. Logic. overhead. Mar. ...

[www.caip.rutgers.edu/~bushnell/COURSE/lec23.ppt](#) - [Similar pages](#)

### [PDF] [DO NOT COPY DO NOT COPY DO NOT COPY DO NOT COPY DO NOT COPY DO NOT COPY DO NOT ...](#)

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... TTL positive-edge-triggered D flip-flops do not use the **master-slave latch** design of ...  
 7.2.7 **Scan Flip-Flop** An important **flip-flop** function for ASIC testing is so ...

[www.ddpp.com/DDPP3\\_mkt/c07samp1.pdf](#) - [Similar pages](#)

### [PPT] [Slide 1](#)

 File Format: Microsoft Powerpoint 97 - [View as HTML](#)

 ... Note that Qs does not change if Dm changes because the **master latch** is closed leaving Qm fixed. ... Edge triggered D **flip-flop** with enable. **Scan Flip-Flop**. ...

[www.ece.lsu.edu/desouza/Classes/EE2730/EE2730%20Set%201.ppt](#) - [Similar pages](#)

### [PDF] [EE241 - Spring 2000 Latch versus Flip-Flop](#)

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... c Types of Flip-Flops **Latch** Pair (**Master-Slave**) D Clk Q D ... Integration of the logic into **flip-flop** • Multiplexed or clock **scan** • Crosstalk insensitivity ...

[bwrc.eecs.berkeley.edu/Classes/icdesign/ee241\\_s00/LECTURES/lecture23-latches.pdf](#)  
 - [Similar pages](#)

### [PPT] [Latches, flipflops, sequential PLAs](#)

 File Format: Microsoft Powerpoint 97 - [View as HTML](#)

 ... CMOS edge-triggered D circuit. Two feedback loops (**master** and **slave** latches). Uses transmission gates in feedback loops. Other D **flip-flop** variations. ... **Scan**. ...

[faculty.cs.wvu.edu/johnson/CS%20347/latches.flipflops.seqplas.ppt](#) - [Similar pages](#)

### [Citations: Comparative analysis of master-slave latches and flip ...](#)

 ... as this determines how much impact the **flipflop** has on ... the **latch** can operate as a **flip flop** with the ... example, synthesis inserts buffers in the **scan** chain when ...

[citeseer.ist.psu.edu/context/1165279/0](#) - 23k - [Cached](#) - [Similar pages](#)

### [PDF] [FPCVT in software FPCVT in hardware](#)

 File Format: PDF/Adobe Acrobat - [View as HTML](#)

 ... **flip-flop** with enable • **master-slave SR flip-flop** • **master-slave JK flip** ... with each clock edge) • T **flip-flop** with enable • **scan flip-flop** (used in ...

[www.stanford.edu/class/ee121/handouts/lect07.pdf](#) - [Similar pages](#)

[\[PDF\] EE E6930 Advanced Digital Integrated Circuits](#)File Format: PDF/Adobe Acrobat - [View as HTML](#)... Page 15. Adding **scan** PowerPC 630 **latch** Page 16. ... Is the **master-slave** FF a FF?Pulse Generator Clock Q Q Input Input **Slave Latch** No Clock **Flip-Flop Master** (L 1 ...[www.cisl.columbia.edu/courses/spring-2002/ee6930/handouts/lecture6.pdf](http://www.cisl.columbia.edu/courses/spring-2002/ee6930/handouts/lecture6.pdf) -[Similar pages](#)[\[PDF\] Design for Testability \(DFT\): Design for Testability \(DFT\):](#)File Format: PDF/Adobe Acrobat - [View as HTML](#)

... Either use a separate clock pin – Or use an alternative design for a single clock pin

**Master latch Slave latch** D SD TC CK MUX SFF (**Scan flip-flop**) Q TC CK ...[sina.sharif.edu/~hessabi/Test/lec24.pdf](http://sina.sharif.edu/~hessabi/Test/lec24.pdf) - [Similar pages](#)

Goooooooooooooogle ►

Result Page:    1   2   3   4   5   6   7   8   9   10    [Next](#) [Search within results](#) | [Language Tools](#) | [Search Tips](#) | [Dissatisfied? Help us improve](#)[Google Home](#) - [Advertising Programs](#) - [Business Solutions](#) - [About Google](#)

©2004 Google